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Title:

A PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND A METHOD FOR WRITING THERETO

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TITLE OF INVENTION

A PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND A METHOD FOR WRITING THERETO

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001] The present invention relates to integrated memory circuits. More specifically, it relates to a method for writing data to a programmable conductor random access memory (PCRAM) cell.

2. Description of Prior Art:

[0002] DRAM integrated circuit arrays have existed for more than thirty years and their dramatic increase in storage capacity has been achieved through advances in semiconductor fabrication technology and circuit design technology. The considerable advances in these two technologies have also achieved higher and higher levels of integration that permit dramatic reductions in memory array size and cost, as well as increased process yield.

[0003] A DRAM memory cell typically comprises, as basic components, an access transistor (switch) and a capacitor for storing a binary data bit in the form of a charge. Typically, a charge of one polarity is stored on the capacitor to represent a logic HIGH (e.g., binary "1"), and a stored charge of the opposite polarity represents a logic

LOW (e.g., binary "0"). The basic drawback of a DRAM is that the charge on the capacitor eventually leaks away and therefore provisions must be made to "refresh" the capacitor charge or else the data bit stored by the memory cell is lost.

[0004] The memory cell of a conventional SRAM, on the other hand, comprises, as basic components, an access transistor or transistors and a memory element in the form of two or more integrated circuit devices interconnected to function as a bistable latch. An example of such a bistable latch is a pair of cross-coupled inverters. Bistable latches do not need to be "refreshed," as in the case of DRAM memory cells, and will reliably store a data bit indefinitely as long as they continue to receive supply voltage. However, such a memory cell requires a larger number of transistors and therefore amount of silicon real estate than a simple DRAM cell, and draws more power than a DRAM cell.

[0005] Efforts continue to identify other forms of memory elements which can store data states and do not require extensive refreshing. Recent studies have focused on resistive materials that can be programmed to exhibit either high or low stable ohmic states. A programmable resistance element of such material could be programmed (set) to a high resistive state to store, for example, a binary "1" data bit or programmed to a low resistive state to store a binary "0" data bit. The stored data bit could then be retrieved by detecting the magnitude of a readout voltage supplying a current switched through the resistive memory element by an access device, thus indicating the stable resistance state it had previously been programmed to.

[0006] One particularly promising programmable, bistable resistive material is known as a programmable metalization material, also termed a programmable conductor material. A memory element comprised of such a material has a stable at rest high resistance state, but can be programmed to a stable low resistance state by application of a suitable voltage across the memory element. A reverse voltage of suitable magnitude applied across the memory element can restore the high resistance

state. The low resistance state is caused by growth of a conductive dendrite through or on the surface of the programmable conductor material. A programmable conductor memory element is nonvolatile, in that the low resistance state need not be refreshed, or if refreshing is required, it is over a relatively long period, e.g. days or weeks.

[0007] One exemplary programmable conductor material comprises a chalcogenide glass material having metal ions diffused therein. A specific example is germanium:selenium (Ge_xSe_{1-x}) diffused with silver (Ag) ions. One method of diffusing the silver ions into the germanium:selenium material is to initially evaporate the germanium:selenium glass and then deposit a thin layer of silver upon the glass, for example by sputtering, physical vapor deposition, or other known technique in the art. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 600 nanometers, so that the energy passes through the silver and to the silver/glass interface, to break a chalcogenide bond of the chalcogenide material. As a result, the Ge:Se glass is doped with silver. Electrodes are provided at spaced locations on the chalcogenide glass to apply voltages for writing and reading the memory element.

[0008] Currently, circuitry for writing data to an array of programmable conductor memory elements is being developed. One problem associated with writing a programmable conductor memory element from a high resistance state to a low resistance state is that a driver is used to supply a write voltage at high current, and once the memory element switches to a low resistance state, the high current is still provided by the driver. This results in wasted power.

SUMMARY OF THE INVENTION

[0009] The present invention provides an improved write circuit and method for writing a programmable conductor random access memory (PCRAM) cell which

reduces wasted power. This is accomplished by utilizing energy stored in the parasitic capacitance of a bit line to supply the write voltage for a programmable conductor memory element. A first predetermined voltage is applied to a first terminal of a programmable conductor memory element and a bit line is charged to a second predetermined voltage. An access transistor couples the precharged bit line to a second terminal of the memory element and the first and second voltages are of a magnitude and polarity which cause the memory element to be written to a desired resistance state. If the first predetermined voltage is held constant, the writing of a memory element to a particular resistance representing a binary value can be controlled by using two different voltages for the second voltage. Since no current supplying driver is used to write a memory element, wasted current is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of preferred embodiments of the invention given below with reference to the accompanying drawings in which:

[0011] Fig. 1 depicts a memory array employing a plurality of PCRAM memory cells, in accordance with an exemplary embodiment of the invention;

[0012] Fig. 2 depicts a PCRAM memory cell of Fig. 1;

[0013] Fig. 3A depicts a flowchart describing an operational flow, in accordance with an exemplary embodiment of the invention;

[0014] Fig. 3B depicts a voltage arrangement across the PCRAM memory cell of Fig.1;

[0015] Fig. 4 depicts a memory array employing a plurality of PCRAM memory cells, in accordance with an alternative embodiment of the invention; and

[0016] Fig. 5 depicts a block diagram of a processor-based system containing a PCRAM memory, in accordance with an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0017] The present invention will be described in connection with exemplary embodiments illustrated in Figs. 1-5. Other embodiments may be realized and other changes may be made to the disclosed embodiments without departing from the spirit or scope of the present invention.

[0018] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged. Similarly, the terms "germanium" and "selenium" are intended to include not only elemental germanium and selenium, but germanium and selenium with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as the physical and electrical properties of the germanium or selenium remain unchanged.

[0019] Fig. 1 depicts a memory array 100 having a plurality of row lines 110, 112, 114 and bit (column) lines 116, 118, 120. At each intersection of a row and bin line there is formed a PCRAM cell such as memory cell 122. Each memory cell (e.g., 122) contains an access transistor 124 and a programmable conductor memory element 126. The programmable conductor memory element may be formed of a chalcogenide glass composition of Se:Ge which is doped with Ag. Suitable material composition for

element 126 are described in U.S. Application Serial No. 09/941,544 entitled "Stoichiometry for Chalocogenide Glasses Useful for Memory Devices and Method of Formation," the disclosure of which is incorporated herein by reference. According to an exemplary embodiment of the present invention, germanium:selenium glasses for use as memory elements are selected from a range of germanium:selenium glasses having stoichiometries that fall within a first stoichiometric range R_1 including $Ge_{18}Se_{82}$ (with a maximum atomic percentage of Ag when doped of about 30% or less) continuously to $Ge_{28}Se_{72}$ (with a maximum atomic percentage of Ag when doped of about 20% or less) and which have the general formula $(Ge_{x1}Se_{1-x1})_{1-y1}Ag_{y1}$, wherein $18 \leq x_1 \leq 28$ and wherein y_1 represents the fit silver (Ag) atomic percentage which is the maximum amount which will keep the glass in the glass forming region.

[0020] A first terminal 150 of the programmable conductor memory element 126 is coupled to a common cell plate 128. One source/drain terminal of each access transistor 124 is coupled to a corresponding bit line (e.g., 118) and another source/drain terminal of each access transistor 124 is coupled to a second terminal 152 of the programmable conductor memory element 126. Further, each bit line 116, 118, 120 is coupled to a precharge circuit 130 so that the bit line can be precharged to one of two predetermined values (e.g., at or approximately at Vdd and at or approximately at ground), as will be described below. Also, a parasitic capacitance 132 is shown for the column line (e.g., 118 of Fig. 1) which is utilized to write , for example, the memory cell 122. The parasitic capacitance has a value of about 500 fF, though this value may vary depending on bit line and memory array architecture.

[0021] Turning to Fig. 2, a schematic diagram of memory cell 122 is depicted in somewhat greater detail. Bit line 118 is coupled to a precharge circuit 130 and also coupled to a first source/drain terminal of access transistor 124, as well as to respective first source/drain terminals of a plurality of other access transistors. Access transistor 124, as well as the other access transistors, are depicted as n-type

complementary metal oxide semiconductor (CMOS) transistors. However, access transistor 124 may easily be replaced with a p-type CMOS transistor as long as the corresponding polarities of the other components and voltages are modified accordingly. A first terminal 150 of the programmable memory element 126 is coupled to the common cell plate 128. A second source/drain terminal of transistor 124 is coupled to a second terminal of the programmable conductor memory element 126. As mentioned above, programmable conductor memory element 126 may be made of a Ge:Se chalcogenide glass which is doped with silver, but other programmable conductor materials known to those of ordinary skill in the art may also be used. The programmable conductor memory element 126 is coupled to a common cell plate 128 for a plurality of memory cells. The cell plate 128 is tied to a voltage terminal for providing a predetermined voltage level (e.g., at or approximately at Vdd/2) to the cell plate 128. A gate of each access transistor 124 shown in Fig. 2 is tied to a respective row line 114. When sufficient voltage is applied to a row line, e.g. 114, an associated access transistor 124 is turned on and conducting. The voltages of the row line 114, bit line 118 and cell plate 128 are selected as described below to enable read and write operations of programmable conductor memory element 126.

[0022] Figs. 3A and 3B, respectively, show a flowchart and voltage chart describing a write operation for a memory cell 122 in accordance with an exemplary embodiment of the invention. In this exemplary process flow, the following parameters of the programmable conductor memory cell are presumed: i) that the voltage across an element 126 required to write from a low resistance state to a high resistance state is 0.25V; (ii) that the current required is approximately 10μA; (iii) that the voltage across an element 126 required to write from a high resistance state to a low resistance state is –0.25V; (iv) that the current required is approximately 10μA; (v) that the low resistance state is approximately 10KΩ; and (vi) that the high resistance state is any value grater than 10MΩ. It should be readily apparent that alternative parameters may be selected for the PCRAM cell, depending on the material composition and size of the

programmable conductor memory element 126, without departing from the spirit and scope of the invention.

[0023] Referring to Fig. 3A and Fig. 3B, the write process begins at process segment 300 At segment 302, the bit line, e.g. bit line 118, is initially precharged to at or approximately at either GND or Vdd, depending on whether the cell is to be programmed to a high resistance state or to a low resistance state. If the cell is going to a high resistance state, then the bit line 118 needs to be precharged to ground, and if the cell is going to a low resistance state, then the bit line needs to be precharged to at or approximately at Vdd. Bit line 118 is precharged to a predetermined voltage via precharge circuit 130, respectively coupled to bit line 118. For purposes of this exemplary description, we will assume the bit line voltage is V1, the voltage drop across the access transistor 124 is V2, the voltage across the memory element 126 is V3, the cell plate voltage is V4, and the word line (transistor 124 gate) voltage is V5, as shown in Figure 3B. We will also assume that Vdd is 2.5V. Accordingly the cell plate 128 is tied to a predetermined voltage of V4, which is at or approximately at Vdd/2, e.g. 1.25V. Note the programmable conductor memory element 126 has reversed voltage write polarities V3 depending on whether a memory element is written to a low resistance state where V3 = –.25V or to a high resistance state where V3 = .25V. Also, a write to a high resistance state is also considered an erase operation. Accordingly, if the cell 122 is going to a low resistance state, then it is necessary to precharge the bit line 118 to at or approximately at Vdd. But if the cell is going to a high resistance state, then the bit line 118 needs to be precharged to at or approximately at ground.

[0024] Once the bit line is precharged, a selected row line is fired at process segment 304 by applying a predetermined voltage V5 to that row line. Process segment 300 also shows the cell plate being held at or approximately at Vdd/2. In this example, a predetermined row line voltage V5 of at or approximately at 2.5V (Vdd) is sufficient to turn on the access transistor 124. Since V1 = 2.5V, V4 = 1.25V, and the voltage

drop V2 across the access transistor is approximately 1 volt (i.e., volt plus resistance of transistor). This leaves a voltage V3 of .25V across the memory element 126 which is sufficient to program it from a high resistance to low resistance state, or keep a previously programmed low resistance state intact.

[0025] If the bit line 118 is precharged to V1 at or approximately at ground, and the voltage drop V2 across the transistor is approximately .2V, then the voltage V3 across memory element 126 is –1.05V, which is sufficient to program it from a low resistance to a high resistance state (also termed an erase) or keep a previously programmed high resistance state intact.

[0026] Process segment 308 indicates that the applied voltage across the memory element 126 which is discharged through the memory element to write the selected resistance value therein. By using the parasitic capacitance 132 of the bit line 118 to hold the precharge voltage, the need to drive the bit line 118 with a transistor connected to a voltage source is obviated, reducing current consumption during a write operation. Finally, at processing segment 310, bit line 118 at the end of the write operation voltage settles to a value which is less than the applied cell plate voltage V4, e.g. < at or approximately at Vdd/2.

[0027] In order to read the contents of the memory cell 122, or more specifically, in order to read the resistance of the programmable conductor memory element 126 of the memory cell 122, a voltage difference of less than + 0.25V is applied across the programmable conductor memory element 126. For example, a voltage of .2V can be used for a read operation. This can be achieved by suitable selection voltage during a read operation. For example, a bit line 118 voltage V1, of 2.45V and a voltage drop V2 of 1 volt will produce .2 volts across memory element 126.

[0028] Referring now to Figure 4, a memory array 400 employing a plurality of programmable conductor memory cells 122 is shown comprising parasitic

capacitance 132, as well as a capacitor 134 and transistor 136. Those items previously described with reference to Fig.1 have the same reference number and will not be described here. Capacitor 134 is added to the column line 118 to provide additional capacitance if the parasitic capacitance on the column line 118, for example, provided by capacitance 132, is not sufficiently high enough to store the precharge voltage. Hence, one or more additional capacitors 134 can be provided as needed for a write operation. Transistor 136 is enabled prior to or at the time of a precharge operation to couple one or more added capacitors 134 to the bit line 118. After a write operation, transistor 136 is turned "off" to keep the extra capacitance off the bit line 118 in order to not interfere with the timing of other operations of the memory array 100.

[0029] Fig. 5 illustrates a block diagram of a processor system 500 containing a programmable conductor random access semiconductor memory as described in connection with Figs. 1-4. For example, the PCRAM memory array 100 described in connection with Figs. 1-4 may be part of random access memory (RAM) 508 which may be configured as a plug-in memory module. The processor-based system 500 may be a computer system or any other processor system. The system 500 includes a central processing unit (CPU) 502, e.g., a microprocessor, that communicates with floppy disk drive 512, CD ROM drive 514, and RAM 508 over a bus 520. It must be noted that the bus 520 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 520 has been illustrated as a single bus. An input/output (I/O) device (e.g., monitor) 504, 506 may also be connected to the bus 520, but are not required in order to practice the invention. The processor-based system 500 also includes a read-only memory (ROM) 510 which may also be used to store a software program. Although the Fig. 5 block diagram depicts only one CPU 502, the Fig. 5 system could also be configured as a parallel processor machine for performing parallel processing.

[0030] While the invention has been described in detail in connection with preferred embodiments known at the time, it should be readily understood that the invention is not limited to the disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. For example, although the invention has been described in connection with specific voltage levels, it should be readily apparent that voltage levels very different than those described herein can be used. Also, although the invention has been described in connection with a specific polarity for the memory element 126, that polarity may be reversed resulting in different voltage levels being applied to the transistor, cell plate, and digit line for a write operation as understood by those skilled in the art. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.